layer **14**. In the embodiment **10**B from FIG. **3**, this deep implantation is performed after the patterning of the thick oxide **34**A, before the formation of the gate. The buffer layer **38** serves to suppress the well documented short channel effects by helping to ensure that the depletion region does not reach too far into the channel.

In the embodiment of FIG. **3**, the breakdown location is still dependent in part on the thickness of epitaxial layer **14** and on the doping concentration of the substrate **12**. Turning to the embodiment **10**C of FIG. **4**, the buffer layer **38** is replaced with thinner p-buffer layer **38**C and second buffer layer **40** having dopant concentration N. In this double deep implant buffer construction, the breakdown location is advantageously located at or around the P-N junction between buffer layer **38**C and buffer layer **40**, making the breakdown location largely independent of the thickness of the epitaxial layer and the dopant concentration of the substrate **12**. The deep implantation of N dopants (preferably Phosphorous) to form the second buffer layer **40** is performed at the beginning of the process flow, after the deposition of the epitaxial layer **14**.

FIG. **5** illustrates the edge termination at the peripheral cells of the device of FIG. **2**, so no gate is shown. The structure of the edge termination is important from a design perspective because it closes the P-N junction in a manner assuring the target breakdown voltage. The illustrated edge termination region surrounds the active area of the transistor (s) created by P-well **16**. It should be understood that a single die can have a plurality of identical transistor cells as described above fabricated in parallel and operating as a single transistor in, for example, a power switch. The source metal **28**A extends beyond the P-well **16** and acts as a field plate (which affects the breakdown voltage in this region of the device), as described above in connection with FIG. **2**. The insulation layer underneath the field plate portion of layer **28**A (again illustrated by reference number **35**) has a thickness between about 0.2-0.5 μm like thicker oxide portion **35** of insulation layer **34**A shown in FIGS. **2-4**. The drain plug **24** is formed at, or proximate to, the edge of the singulated die having the transistor formed therein, i.e., the die is singulated from adjacent dies on a wafer at or proximate to the drain plug **24**. The edge termination region ends with drain plug **24** separating the transistor from the edge of the singulated die. This illustrated structure is the natural consequence of the formation of the structure of FIG. **2**.

In a preferred embodiment, the background doping of the epitaxial layer is 1×10^{16} atoms/cm^3, the P-well **16** is formed by overlapping deep buffer **38** and body **16** implantations and the distance between the P-well and the drain plug is 1.5 μm. This edge termination can support breakdown voltages higher than 35V.

In an exemplary application, the improved power LDMOS device is fabricated in parallel with a plurality of other similarly structured devices and packaged for use as a power transistor in, for example, a DC/DC voltage regulator.

FIGS. **6-10** show electrical characteristics obtained by numeric simulation of a 20V device **10** of FIG. **4** with an active area of 1 mm^2 designed for a maximum breakdown voltage of 20V and a maximum allowed source-to-gate voltage of 12V, with a gate thickness of 300 Å. FIG. **6** shows drain current as a function of the drain voltage at Vgs equal to 2.0, 2.5, 3.0, 4.0 and 5.0 volts. The flat Ids curve in saturation region (Vds>1V) shows the transistor is free of short channel effects.

FIG. **7** shows the resistance of a device with an active area of 1 mm^2 calculated as a function of the gate voltage for the drain voltage of 0.1V. It can be seen that the resistance predicted for Vgs equal to 4.5V is about 13 mΩ*mm^2, whereas the resistance of similar devices in the art is higher than 20 mΩ*mm^2.

FIG. **8** shows the drain current as a function of the gate voltage for a drain voltage of 5V. It can be seen that the threshold voltage of the transistor is kept at a low value below 1.5V, which is advantageous for power applications. In contrast, modern power MOSFETs with short channel lengths usually result in a much higher threshold voltage of more than 2.2V to keep the device free of short channel effects.

FIG. **9** shows the capacitances Ciss, Coss and Crss as a function of the drain voltage, where Ciss is the input capacitance (Cgs+Cgd), Coss is the output capacitance (Cds+Cdg) and Crss is the feedback capacitance (Cdg). Cdg is very close to Cgd, depending on to what terminals the source signals are applied and at what terminals the response signals are measured. Generally speaking, the proposed device has smaller capacitances than the commercially available products. Particularly, the feedback capacitance Crss (approximately equal to Cgd) is smaller by a factor of 5 than similar existing power MOSFETS.

Finally, FIG. **10** shows a gate charge curve. It can be seen from the curve that that a gate voltage of 5V can be reached by charging the gate with only 2.2 nC/mm^2. This is a very low charge providing an accepted figure of merit of Rds (Vgs=10V)*Qg(VS=5V) of 22 mΩ*nC, whereas the similar devices in the art result in values higher than 50 mΩ*nC.

As set forth above, an improved power LDMOS device is provided having an n-channel transistor formed over a low resistance N-substrate. The device exhibits low on-resistance ($R_{ds\text{-}on}$) by lowering the resistive contribution of the substrate and low Cgd capacitance by minimizing the electrostatic coupling between the gate and drain electrodes. In embodiments, the source contact extends over gate and drain regions, thereby providing a high current capability.

Although the invention has been described in terms of exemplary embodiments, it is not limited thereto. Rather, the appended claims should be construed broadly to include other variants and embodiments of the invention that may be made by those skilled in the art without departing from the scope and range of equivalents of the invention.

What is claimed is:

1. A lateral metal-oxide-semiconductor transistor device comprising:

a substrate having a first conductivity type and having a lightly doped epitaxial layer thereon having an upper surface;

source and drain regions of the first conductivity type formed in the epitaxial layer proximate the upper surface, said source and drain regions being spaced from one another and having a channel region of a second conductivity type formed therebetween in said epitaxial layer, said channel region extending under said source region;

a conductive gate formed over a gate dielectric layer formed over said channel region and partially overlapping said source and drain regions;

a drain contact electrically connecting said drain region to said substrate and spaced from said channel region comprising:

a first trench formed from the upper surface of said epitaxial layer to said substrate and having a side wall along said epitaxial layer;

a highly doped region of said first conductivity type formed along said side wall of the first trench; and